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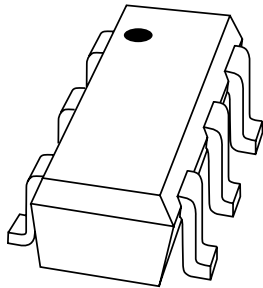
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Kind regards,

Team Nexperia

# DATA SHEET



## **PUMF12**

**PNP general purpose transistor;  
NPN resistor-equipped transistor**

# PNP general purpose transistor; NPN resistor-equipped transistor

## PUMF12

### FEATURES

- General purpose transistor and resistor equipped transistor in one package
- 100 mA collector current
- 50 V collector-emitter voltage
- 300 mW total power dissipation
- SOT363 package; replaces two SOT323 (SC-70) packaged devices on same PCB area
- Reduced pick and place costs.

### APPLICATIONS

- Power management switch for portable equipment, e.g. cellular phone and CD player
- Switch for regulator.

### DESCRIPTION

PNP general purpose transistor and an NPN resistor-equipped transistor in a SOT363 (SC-88) plastic package.

### MARKING

TYPE NUMBER	MARKING CODE <sup>(1)</sup>
PUMF12	R2*

### Note

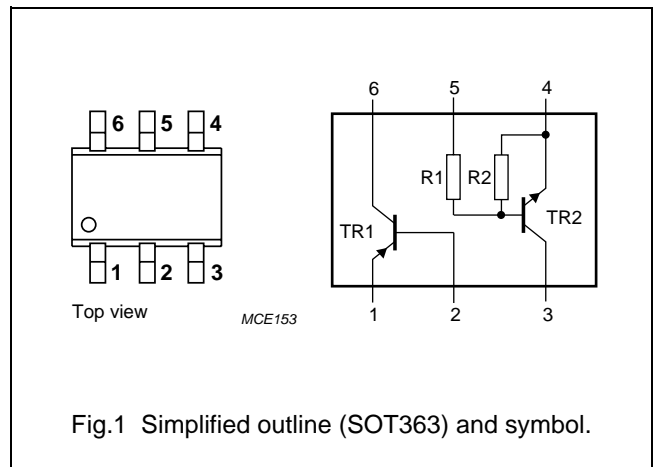
1. \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
<b>TR1 (PNP)</b>			
$V_{CEO}$	collector-emitter voltage	-50	V
$I_C$	collector current (DC)	-100	mA
$I_{CM}$	peak collector current	-200	mA
<b>TR2 (NPN)</b>			
$V_{CEO}$	collector-emitter voltage	50	V
$I_O$	output current (DC)	100	mA
R1	bias resistor	22	k $\Omega$
R2	bias resistor	47	k $\Omega$

### PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



# PNP general purpose transistor; NPN resistor-equipped transistor

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor</b>					
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	200	mW
$T_{stg}$	storage temperature range		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C
<b>TR1 (PNP)</b>					
$V_{CBO}$	collector-base voltage	open emitter	–	–50	V
$V_{CEO}$	collector-emitter voltage	open base	–	–40	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–100	mA
$I_{CM}$	peak collector current		–	–200	mA
<b>TR2 (NPN)</b>					
$V_{CBO}$	collector-base voltage	open emitter	–	50	V
$V_{CEO}$	collector-emitter voltage	open base	–	50	V
$V_{EBO}$	emitter-base voltage	open collector	–	10	V
$V_i$	input voltage				
	positive		–	+40	V
	negative		–	–10	V
$I_o$	output current (DC)		–	100	mA
$I_{CM}$	peak collector current		–	100	mA
<b>Per device</b>					
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	300	mW

### Note

1. Device mounted on an FR4 printed-circuit board.

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	416	K/W

### Note

1. Device mounted on an FR4 printed-circuit board.

PNP general purpose transistor; NPN resistor-equipped transistor

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CHARACTERISTICS

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>TR1 (PNP)</b>						
I <sub>CBO</sub>	collector cut-off current	V <sub>CB</sub> = -30 V; I <sub>E</sub> = 0	-	-	-100	nA
		V <sub>CB</sub> = -30 V; I <sub>E</sub> = 0; T <sub>j</sub> = 150 °C	-	-	-10	μA
I <sub>EBO</sub>	emitter cut-off current	V <sub>EB</sub> = -4 V; I <sub>C</sub> = 0	-	-	-100	nA
V <sub>CEsat</sub>	saturation voltage	I <sub>C</sub> = -50 mA; I <sub>B</sub> = -5 mA; note 1	-	-	-200	mV
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -6 V; I <sub>C</sub> = -1 mA	120	-	-	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = -12 V; I <sub>E</sub> = i <sub>e</sub> = 0; f = 1 MHz	-	-	2.2	pF
f <sub>T</sub>	transition frequency	V <sub>CE</sub> = -12 V; I <sub>C</sub> = -2 mA; f = 100 MHz	100	-	-	MHz
<b>TR2 (NPN)</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0	-	-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0	-	-	1	μA
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0; T <sub>j</sub> = 150 °C	-	-	50	μA
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0	-	-	120	μA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 5 mA	80	-	-	
V <sub>CEsat</sub>	saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 0.5 mA	-	-	150	mV
V <sub>i(off)</sub>	input off voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA	-	0.9	0.5	V
V <sub>i(on)</sub>	input on voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 2 mA	2	1.1	-	V
R1	input resistor		15.4	22	28.6	kΩ
$\frac{R2}{R1}$	resistor ratio		1.7	2.1	2.6	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = i <sub>e</sub> = 0; f = 1 MHz	-	-	2.5	pF

Note

1. Device mounted on an FR4 printed-circuit board.

APPLICATION INFORMATION

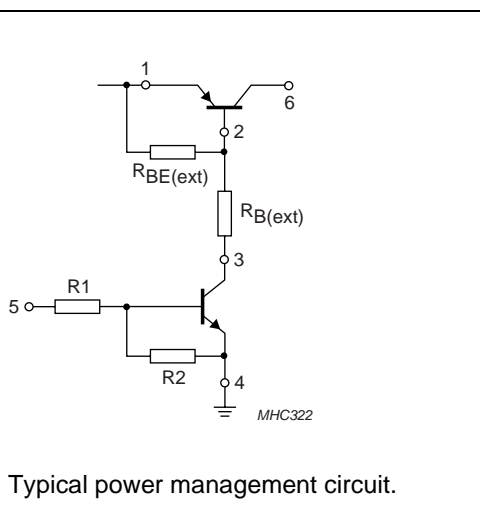


Fig.2 Typical power management circuit.

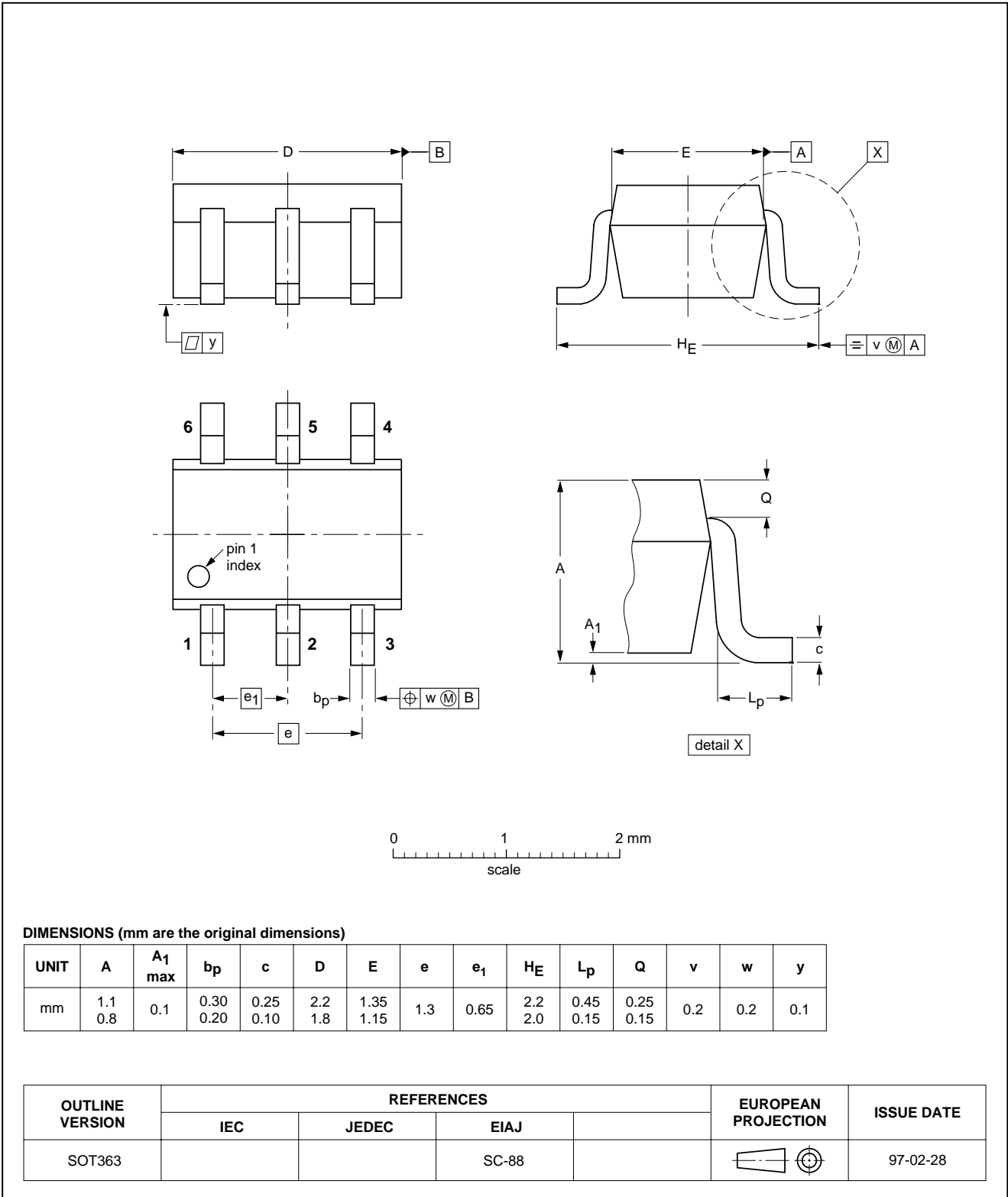
PNP general purpose transistor; NPN resistor-equipped transistor

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



PNP general purpose transistor; NPN resistor-equipped transistor

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**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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# ***NXP Semiconductors***

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## **Contact information**

For additional information please visit: **<http://www.nxp.com>**

For sales offices addresses send e-mail to: **[salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)**

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